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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/705,972	11/13/2003	Norio Nakamura	245445US2S	6778
22850	7590	05/25/2006	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314				KOVALICK, VINCENT E
ART UNIT		PAPER NUMBER		
				2629

DATE MAILED: 05/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/705,972	NAKAMURA, NORIO	
	Examiner	Art Unit	
	Vincent E. Kovalick	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 13 November 2003.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1,2 and 5 is/are rejected.
- 7) Claim(s) 3 and 4 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 13 November 2003 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 11/23/05
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____.

DETAILED ACTION

1. This Office Action is in response to Applicant's Patent Application, Serial No. 10/705,972, with a File Date of November 13, 2003.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasai (Pub. No. US 2003/0058199) taken with Okada (JP62064599)

Relative to claim 1, Kasai teaches current generating circuit, electro-optical device and electronic apparatus (pgs. 1 & 2, paras. 0009-0025); Kasai further teaches a display device comprising: a plurality of self-luminous elements arrayed to form a display screen; and a driving circuit which causes drive currents to flow in said self-luminous element according to pixel signals (pg. 1, para. 0006; pg. 2, paras. 0019-0024) and Fig. 1).

Kasai does not teach a driving circuit being configured to restrict the drive currents flowing in said self-luminous elements upon increases in the total sum of the drive currents.

Okada **teaches** a drive circuit for light emitting elements (Purpose); Okada further **teaches** a driving circuit being configured to restrict the drive currents flowing in said self-luminous elements upon increases in the total sum of the drive currents (Abstract).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Kasai the feature as taught by Okada in order to put in place the means necessary to regulate the current flow to the self-luminous elements that make-up the display device.

Regarding claim 5, Kasai further **teaches** the said display device wherein said self-luminous elements are formed of organic electroluminescence elements (pg. 1, para. 0006).

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kasai taken with Okada as applied to claim 1 in item 3 hereinabove, and further in view of Koyama (Pub. No. US 2002/0113763) still further in view of Imawaka Pub. No. (JP411352936 taken with Shibata (Pub. No. JP410319373)

Regarding claim 2, Kasai taken with Okada **does not teach**; a display device wherein said driving circuit comprises; a D/A conversion circuit which digital –to-analog converts the pixel signals; a gradation reference circuit which generates a predetermined number of gradation reference signals which are referred to by said D/A conversion circuit; and a correction circuit which detects the total sum of the drive currents flowing in said self-luminous elements and controls said gradation reference circuit to produce a predetermined number of gradation reference signals whose levels are uniformly corrected according to the total sum.

Koyama **teaches** a Liquid Crystal Display device and method of driving the same

(pg. 2, para. 0035; pg. 3, paras. 0036-0048 ; and Fig. 1A); Koyama further **teaches** a display device wherein said driving circuit comprises; a D/A conversion circuit which digital-to-analog converts the pixel signals (pg. 7, paras. 0150- 0152).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Kasai taken with Okada the feature as taught by Koyama in order to provide the display pixel signals in the proper format.

Kasai taken with Okada in view of Koyama **does not teach** a gradation reference circuit which generates a predetermined number of gradation reference signals which are referred to by said D/A conversion circuit; and a correction circuit which detects the total sum of the drive currents flowing in said self-luminous elements and controls said gradation reference circuit to produce a predetermined number of gradation reference signals whose levels are uniformly corrected according to the total sum.

Imawaka **teaches** intermediate gradation display control unit and method for liquid crystal display (Problem to be Solved); Imawaka further **teaches** a gradation reference circuit which generates a predetermined number of gradation reference signals which are referred to by said D/A conversion circuit (Abstract).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Kasai taken with Okada in view of Koyama the feature as taught by Imawaka in order to provide the selection of gradation reference signals necessary to assure the proper current levels to the display pixels.

Kasai taken with Okada in view of Koyama and further in view of Imawaka **does not teach** a correction circuit which detects the total sum of the drive currents flowing in said

self-luminous elements and controls said gradation reference circuit to produce a predetermined number of gradation reference signals whose levels are uniformly corrected according to the total sum.

Shibata teaches a Liquid Crystal Display Device and System (Problem to be Solved);

Shibata further teaches a correction circuit which detects the total sum of the drive currents flowing in said self-luminous elements and controls said gradation reference circuit to produce a predetermined number of gradation reference signals whose levels are uniformly corrected according to the total sum.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Kasai taken with Okada in view of Koyama and further in view of Imawaka the feature as taught by Shibata in order to provide the desired current levels to the display pixels.

Allowable Subject Matter

5. Claims 3 and 4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Relative to claim 3, the major difference between the teachings of the prior art of record (Pub. No. US 2003/0058199. Kasai and Pub. No. JP 63229791) and that of the instant invention is that said Prior Art of record **does not teach** a display device wherein a gradation reference circuit includes a voltage division circuit which comprises a plurality of resistor elements connected to output a predetermined number of gradation

reference voltages whose voltage ratios to a reference power supply voltage differ from each other, as the predetermined number of gradation reference signals, respectively.

Regarding claim 4, the major difference between the teachings of the said prior art of record and that of the instant invention is that said Prior Art of record **does not teach** a display device wherein the gradation reference circuit includes a current mirror circuit which comprises a plurality or active current mirror elements connected to output predetermined number of gradation reference currents whose current ratios to a reference power supply current differ from each other, as the predetermined number of gradation reference signals, respectively.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U. S. Patent No. 5,706,020 Iwsama

U. S. Patent No. 4,812,642 Hasegawa et al.

U. S. Pub. No. US 2001/0043113 Hoshino et al.

To Respond

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent E. Kovalick whose telephone number is 571-272-7669. The examiner can normally be reached on Monday-Thursday 7:30- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Vincent E. Kovalick
May 19, 2006



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SUPERVISORY PATENT EXAMINER
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